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Guideline for Reverse Bias Reliability Evaluation Procedures for Gallium Nitride Power Conversion Devices

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**GUIDELINE FOR REVERSE BIAS RELIABILITY EVALUATION
PROCEDURES FOR GALLIUM NITRIDE POWER CONVERSION DEVICES**

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Foreword

High Temperature Reverse Bias testing of a GaN power conversion product is typically performed during product qualification, qualification of a new technology or design, or as part of on-going reliability testing.

GUIDELINE FOR REVERSE BIAS RELIABILITY EVALUATION PROCEDURES FOR GALLIUM NITRIDE POWER CONVERSION DEVICES

(From JEDEC Board Ballot JCB-23-43, formulated under the cognizance of JC-70.1 Subcommittee on GaN Power Electronic Conversion Semiconductor Standards.)

1 Scope

This publication presents guidelines for evaluating the Time Dependent Breakdown (TDB) reliability of GaN power switches. It is applicable to planar enhancement-mode, depletion-mode, GaN integrated power solutions and cascode GaN power switches. If the GaN power component used in a GaN integrated power solution has been tested by HTRB either individually or as part of the integrated power solution, then this guideline will be met.

This guideline will cover suggested stress conditions and related test parameters for evaluating the TDB reliability of GaN power transistors using off-state bias. These stress conditions and test parameters are designed to evaluate the reliability performance of GaN products over their useful lifetime under accelerated stress conditions. The stress described in this document is referred to as continuous DC voltage with the device in reverse bias (Off state). Temperature and/or voltage may be used to accelerate the rate of aging mechanisms of the devices.

Methods for determining voltage and temperature acceleration are beyond the scope of this guideline. Suppliers are to provide the data and experimental methods used upon request by the customers and to be in compliance with JESD91. Throughout this guideline, it will be assumed that voltage and temperature acceleration coefficients are known quantities.

In the case of an GaN device integrated with a silicon device this document only applicable to the GaN portion of the device and does not cover off state failure mechanisms of the non-GaN components.

2 Terms

High Temperature Reverse Bias (HTRB) test: A reliability test where a reverse bias voltage is applied across the drain to source at an elevated temperature.

Maximum Operating Voltage: The maximum supply voltage at which a device is specified to operate in compliance with the applicable device specification or data sheet.

Absolute maximum rated voltage: The maximum voltage that may be applied to a device, beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology.

Maximum operating junction temperature: The maximum junction temperature at which a device is specified to operate in compliance with the applicable device specification or data sheet.

Absolute maximum rated junction temperature: The maximum junction temperature of an operating device beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology. Manufacturers may also specify maximum case temperature for specific packages as applicable.

Stress conditions: voltage and temperature applied during HTRB.

Use conditions: voltage and temperature applied during normal device operation as defined in the mission profile or in the datasheet.

Mission Profile: The simplified representation of all of the relevant conditions to which a device will be exposed in its intended application throughout the full life cycle.

t(STRESS): duration of the stress-test under accelerated conditions.

t(USE): duration of the useful life of the device under normal conditions

VDS(STRESS): drain to source voltage applied during the stress-test

VDS(USE): drain to source voltage from mission profile, or under use conditions

T(STRESS): temperature (junction) applied during the stress-test

T(USE): temperature (junction) from mission profile or under use conditions

AFT: temperature acceleration factor between T(STRESS) & T(USE)

AFV: voltage acceleration factor between VDS(STRESS) & VDS(USE)

AFX: total acceleration factor (the product AFT * AFV)

3 References

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

JESD91 “Method for Developing Acceleration Models for Electronic Component Failure Mechanisms”

JESD22-A108 “Temperature, Bias and Operating Life”

JESD47 “Stress Test Qualification of Integrated Circuits”

JESD94 “Application Specific Qualification Using Knowledge Based Test Methodology”

AEC Q101 “Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in Automotive Applications”

4 High Temperature Reverse Bias Stress Conditions (HTRB)

The conditions for HTRB stress-testing are defined when:

- Stress conditions are within the datasheet maximums.
- Stress conditions result in a “worse case” stress situation.
- Acceleration coefficients for potential failure modes may not be known.

VDS(STRESS): voltage required for maximum acceleration of failure modes.

- Typically: Maximum recommended voltage (usually 80% of device rating).
- Lower voltage setting may be appropriate for specific failure modes following the guidance in clause 5.

T(STRESS): Junction temperature required for maximum acceleration of failure modes.

- Typically: Maximum operating junction temperature (see JESD22-A108G).
- Low temperature may be used as a test condition when experimental data supports low temperature as a worse case condition.

$t(\text{STRESS}) \geq 1000$ hours.

5 Application Specific Stress-Testing

In some cases, it may be desirable to apply stresses to the device beyond the requirements defined by the HTRB test.

Conditions that can be considered when modifying HTRB stress conditions:

- Application has a demanding loading profile
- Application has an extended lifetime requirement
- Application has a specific failure rate target over lifetime below the Lot Tolerant Percent Defective (LTPD) range

Temperature, voltage or test duration may be modified from HTRB stress conditions in clause 4 to satisfy any application specific requirements:

- These stress conditions may be “outside” of the datasheet limits
- Stress conditions should not introduce novel failure modes
- Application specific testing may take into account differences between stress and use case (mission profile) conditions.

If the calculated $t(USE)$ for HTRB stress-test is greater than the $t(USE)$ as defined in the mission profile the standard HTRB test is sufficient.

- The calculations are as follow:
 - $AFX = (AFT * AFV)$: Total acceleration factor for HTRB stress-test relative to mission profile.
 - $t(USE) = AFX * t(STRESS)$: this defines the total use time under stress conditions.

Refer to JESD91 for guidance in defining acceleration factors and coefficients.

6 Considerations when Defining Mission Profile Accelerated Stress Conditions

Stress conditions should avoid accelerating failure modes that would not typically be experienced under normal use conditions. Stress conditions should also avoid the wear out portion of the bathtub curve. Self-heating of the device during this stress-test should be taken into account.

- It is recommended that stress duration should not be much shorter than 500-1000 hours to avoid introducing atypical failure modes. Voltage and/or temperature values can be adjusted to meet this requirement.
- It is possible that different combinations of temperature and/or voltage can result in the same stress duration.
 - Not all stress conditions will be at datasheet maximums or beyond...example: voltage beyond datasheet maximum may be used, but temperature may be kept a nominal operating condition.

Refer to Appendix 7 of AEC Q101 Rev D1 for guidance on how to determine appropriate voltage, temperature and stress-test durations.

7 Measurements, Reporting, and Sample Sizes

Electrical testing shall be completed as soon as possible after removal of bias from devices. It is recommended that tests be run within 72 hours. Bias should remain on devices under stress until temperatures of the Device Under Test (DUT) are decreased to where they are removed for electrical readouts. If the availability of test equipment or other factors makes meeting this recommendation difficult, bias must be maintained on the devices; this may be either at the stress temperature or room temperature and the bias may be reduced to the typical target voltage application from any accelerated voltage in use for stress [per JESD22-A108G].

Lot sizes and acceptable failure numbers are based upon an acceptable LTPD level as defined clause 3.8 of JESD47. Samples should be taken from three separate wafer fab lots.

The stress-test report should include, sample size, test conditions (voltage, temperature) acceleration factors, and mission profile (if applicable).

8 Failure Criteria

The criteria for failure are;

- a) Catastrophic failure, or
- b) Any devices that drifted out of specification defined in the product datasheet limits.

Annex A (Informative) Revision History

Revision	Changes	Date of Release
	Initial Release	



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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

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